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PATENT APPLICATION

ATTORNEY DOCKET NO. 200310369-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Ruben W. Castelino, John A. Kowaleski, Jr. **Confirmation No.:**

Application No.: N/A **Examiner:** Not assigned

Filing Date: Herewith **Group Art Unit:**

Title: POSITION REFERENCE BEACON FOR INTEGRATED CIRCUITS

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

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I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

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Typed Name: **Michael G. Verga**

Respectfully submitted,

Ruben W. Castelino, John A.

By _____

Michael G. Verga, Esq.
Attorney/Agent for Applicant(s)
Reg. No. **39,410**

Date: **11/03/03**

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PTO/SB/08a/b (08-03)
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Substitute for form 1449A/B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	Not Yet Assigned
Filing Date	Herewith
First Named Inventor	Ruben Castelino, et al.
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	200310369-1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	5,940,545	08/99	Kash et al.	
	AB	6,469,529	10/02	Bruce et al.	
	AC	6,576,966	06/03	Bulucea	
	AD	6,587,994	07/03	Yamaji	
	AE	6,610,565	08/03	Kim et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Country	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	BA					

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	W. J. ROESCH, "*Light Emission as an Analysis Tool for GaAs ICs*", Triquint Semiconductor, Inc., pgs. 1-5;	"
	CB	Andrea PACELLI, "*Modeling of MOSFET hot carrier effects*", SUNY at Stony Brook, Department of Electrical and Computer Engineering, ESE 514 pgs. 1-9 (2001);	
	CC	"*Picosecond imaging Circuit Analysis*", IBM Research, Press Releases pgs.1-3;	
	CD	Malgorzata CHRZANOWSKA-JESKE, "*Between Failure, Reliability, Yield and IC Layout*", Portland State University, Electrical and Computer Engineering, pgs.1-9 (2003);	
	CE	Zhihong LIU, "*Hot Carrier Effect—A Fading Concern or a Growing Problem?*" Viewpoint, EEdesign Editorial, pgs. 1-4 (1998);	
	CF	Yusuf LEBLEBICI, "*Design Considerations for CMOS Digital Circuits with Improved Hot-Carrier Reliability*", *IEEE Journal Of Solid-State Circuits, Vol:31, No.7 (1996);*	
	CG	S. MAHAPATRA, et al., "*Device Scaling Effects on Hot-Carrier Induced Interface and Oxide-Trapped Charge Distributions in MOSFET's*", *IEEE Transactions On Electron Devices, Vol.47, No. 4 (2000).*	

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Examiner Signature		Date Considered	